Amendments to the Specification

Please replace the Title with the following Title:

APPARATUS IN A MICROPROCESSOR FOR BRANCHING IN RESPONSE TO AN INSTRUCTION CACHE FETCH ADDRESS WITHOUT KNOWING WHETHER OR NOT A BRANCH INSTRUCTION IS PRESENT IN A CACHE LINE OF INSTRUCTION BYTES SELECTED FROM THE INSTRUCTION CACHE BY THE FETCH ADDRESS AND FOR CORRECTING IF THE BRANCHING WAS ERRONEOUS

Please replace the table on page 1 with the following amended table:

Docket #	Serial #	Title
CNTR:2021	09/849736	SPECULATIVE BRANCH TARGET ADDRESS CACHE
CNTR:2023	09/849734	SPECULATIVE HYBRID BRANCH DIRECTION PREDICTOR
CNTR:2050	09/849822	DUAL CALL/RETURN STACK BRANCH PREDICTION SYSTEM
CNTR:2052	09/849799	SPECULATIVE BRANCH TARGET ADDRESS CACHE WITH SELECTIVE OVERRIDE BY SECONDARY PREDICTOR BASED ON BRANCH INSTRUCTION TYPE
CNTR:2062	09/849754	APPARATUS AND METHOD FOR SELECTING ONE OF MULTIPLE TARGET ADDRESSES STORED IN A SPECULATIVE BRANCH TARGET ADDRESS CACHE PER INSTRUCTION CACHE LINE
CNTR:2063	09/849800	APPARATUS AND METHOD FOR TARGET ADDRESS REPLACEMENT IN SPECULATIVE BRANCH TARGET ADDRESS CACHE